The ARM® RealView® Versatile family of development boards provide a feature rich prototyping system for system-on-chip designs. This family includes the first development board to support both the ARM926EJ-S™ PrimeXsys™ Platform, and a range of integrated high performance IP such as PowerVR’s MBX 3D graphics acceleration technology.

The high performance Versatile family enhances the end-user experience for benchmarking and application development. It simplifies hardware and software development, which shortens time to market.

The RealView Versatile family complements the existing RealView Integrator™ family by offering an alternative balance of flexibility versus performance. The performance critical parts of a system have been combined into a highly integrated development chip to enable ASIC emulation and software development at near to real system speed. The development chip includes three off-chip bus interfaces to maintain flexibility in user defined expansion.

The Versatile family comprises:
- The Versatile Platform Baseboard for ARM926EJ-S
- RealView Logic Tiles
- RealView Analyzer Tile
- RealView Interface Tiles

The first baseboard in the Versatile family is the RealView Versatile Platform Baseboard for ARM926EJ-S. This board has been designed specifically for ASIC emulation and prototyping, and supports advanced 3D graphics application development around ARM and PowerVR MBX cores. It is an ideal development board for the ARM926EJ-S PrimeXsys developer community.

The RealView Versatile Platform Baseboard provides an AMBA™ Multi-layer AHB prototyping environment. At the heart of the board is a highly integrated development chip which is based on the ARM926EJ-S PrimeXsys Platform architecture. External bus interfaces on the development chip, which enable bus layers inside the chip to be routed off-chip, provide access to the multiple internal bus layers of the PrimeXsys Platform architecture for expansion.

Features of the Development Chip
- ARM926EJ-S processor, Jazelle® Java acceleration hardware and DSP extensions
- PowerVR MBX 3D Graphics accelerator
- MOVE™ coprocessor, hardware acceleration for MPEG encode
- Vector Floating Point (VFP) coprocessor, hardware assist for floating point arithmetic
- Off-chip AHB bridges and system monitor for cycle accurate system prototyping
- Memory sub-system including DMA controller with a choice of static and dynamic memory and boot options
- Vectored interrupt controller
- Peripherals essential for operating system support, including JTAG run-control and Trace ports

Performance
- CPU to 210MHz
- Memory bus, MBX and internal AHB to 75MHz (typical maximum figures at room temperature)

Development Chip Block Diagram

The development chip integrates high performance IP such as memory and DMA controllers and the ARM VFP9-S coprocessor around the ARM926EJ-S core. The vector processing capability of the ARM VFP9-S coprocessor offers increased performance for imaging applications such as scaling, 2D and 3D transforms, font generation, and digital filters. The development chip also includes an implementation of the ARM MOVE coprocessor which significantly improves the motion estimation capability required for applications like MPEG encode through hardware assistance for sum-of-absolute-differences (SAD) calculations.
RealView Versatile Platform Baseboard for ARM926EJ-S

Memory
- 64MB NOR Flash
- 64MB Disk-on-chip NAND Flash
- 128MB 32-bit SDRAM
- 2MB SRAM

Peripherals
- Ethernet
- LCD and touchscreen
- VGA monitor output
- 4 x Serial ports
- 1 x Synchronous Serial Port
- 32 GPIO pins
- 1 x USB OTG, 2 x USB Host
- 2 x SmartCard (SIM)
- Keyboard and mouse interfaces
- 2 x MMC/SD Card
- Stereo audio in/out and microphone
- 2 line x 16 character LCD
- Vector interrupt controller
- PCI 32-bit 66MHz host controller
- Built-in JTAG run-control hardware

Supported OS
- WinCE
- SymbianOS
- ARM Embedded Linux
- ThreadX
- …and others in development

Compatible boards
- RealView Logic Tile, LT-XC2V6000
- RealView Logic Tile, LT-XC2V8000
- RealView Analyzer Tile
- RealView Interface Tile 1 (2Q 2004)

Options
- Expansion module sites for static and dynamic memory
- Logic Tile expansion sites for peripherals and secondary processors
- PCI backplane, 3 slots, clock generation and arbitration
- Choice of LCD panels including 3.8” QVGA and 8.4” VGA

Support CD
Firmware
- System and memory initialization code
- Polled serial drivers
- Real-time clock (time function) in retargeted C library
- Disk-on-Chip, NAND flash file system
- NOR Flash memory read, write and erase code
- Serial and Ethernet image transfer to memory
- PCI Library
- ScanPCI utility
- Little and big-endian build options
- Vectored interrupt controller example
- Timer example
- Hardware vector floating point (VFP) example
- Functional test program for all peripherals
- C library support for stand-alone and semi-hosted images
- Simple makefiles
- Little and big-endian build options

Pre-built binaries
- Boot monitor
- Functional test program
- ARM Embedded Linux 2.4
- SymbianOS 7s

Hardware
- Verilog RTL for baseboard FPGA

Documentation
- Versatile Platform Baseboard for ARM926EJ-S User Guide
- ARM926EJ-S Development Chip Reference Manual
- PrimeCell® Peripheral Technical Reference Manuals
Example Applications

Example 1: A Logic Tile is used to add a synthesisable DSP as a second processor on the Versatile Platform Baseboard. One master port on the development chip routes to the PCI interface and peripherals inside the baseboard FPGA and the other master port routes to the DSP sub-system, through a shared memory with mailboxes. The DSP accesses the memory controllers inside the development chip through an AMBA AHB interface to the slave port.

Example 2: A camera is attached to the platform using a Logic Tile and peripheral I/O board on the top of the stack. The camera is an AMBA AHB slave, but uses the DMA controller in the development chip to transfer image data stored in RAM on the Logic Tile to SDRAM on the baseboard.

RealView Logic Tiles

Features
- Small form factor, 88mm x 119mm
- High density, robust header connectors
- Stack multiple tiles to create very large prototyping systems
- Interfaces directly to Versatile Platform for multi-layer designs
- Supplied with example RTL and test software
- Stacking height 8mm
- Supports many IO standards such as LVTTL and LVCMOS

Details
- Xilinx VirtexII, XC2V6000 or XC2V8000 FPGA
- 2 x 2MB ZBT SRAM
- 3 x Programmable clock generators
- 4 LEDs
- 4-way DIL switch
- Push button
- Configuration flash memory for 2 images and loader PLD

Input/Output Connections
- 395 IO up, 395 IO down
- 128 IO common bus
- Switching to increase downwards facing IO to ~600

RealView Analyzer Tile

Features
- Allows visibility of signals between tiles in a stack
- 20 Mictor Logic Analyzer connectors
- Test points for clocks

Ordering Information

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<td>RealView Logic Tile LT-XC2V6000</td>
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<td>INLT8-BD-0196A</td>
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The ARM® RealView® family of feature rich development boards provides an excellent environment for prototyping system-on-chip designs. Through a range of plug-in options, hardware and software applications can be developed and debugged.

The high performance Versatile family enhances the end-user experience for benchmarking and application development. It simplifies hardware and software development, which shortens time to market.

The Platform Baseboard for ARM1176JZF-S is a development board especially designed for ARM V6 architecture and TrustZone® software applications development on a high speed expandable platform.

**Platform Baseboard for ARM1176JZF-S**

The Platform Baseboard for ARM1176JZF-S features a Development Chip including an ARM1176JZF-S processor and all the performance critical components of a standard applications ASIC, such as LCD controller and dynamic and static memory controllers. The development chip also implements CoreSight debug and trace IP, as well as off-chip bridges for prototyping of custom AXI masters and slaves on FPGA. A companion Xilinx Virtex-4 FPGA implements DMA and PCI controllers and low speed peripherals.

The ARM1176JZF-S development chip architecture enables the development of security critical applications, and optimized balanced CPU workload energy consumption applications using TrustZone® technology along with the Intelligent Energy Management (IEM) technology from ARM®.

In order to accelerate software development and reduce time to market the Platform Baseboard is delivered with FPGA bit file and example software. A number of operating systems, including Embedded Linux will also be ported to this board to help users accelerate the development of OS-based applications.
**Specification**

**Platform Baseboard Features**
- ARM1176JZF-S processor at 280MHz
- Intelligent Energy Management (IEM) support
- TrustZone® software and hardware support
- CoreSight ETM11™, CoreSight ETB11™ support
- Virtex-4 XC4VLX40 FPGA
- 128MB Mobile DDR SDRAM, 2MB Cellular RAM
- 128MB NOR Flash
- PISMO expansion site (www.pismoworld.org)
- AXI expansion with Logic Tiles at 35MHz

**Platform Baseboard Peripherals**
- 10/100 Ethernet MAC
- High Speed USB v2.0 OTG controller
- 32-bit 66MHz PCI controller
- 133MHz 32-bit DDR SDRAM controller
- 50MHz 32-bit Cellular SRAM controller
- 50MHz 32-bit NOR Flash controller
- VGA, keyboard and mouse connectors
- SmartCard and Multimedia/SD Card controller
- Stereo audio Line in/out and microphone
- 5 UARTs and character LCD
- Switches, LEDs and GPIO headers

*Note: Speed figures subject to change*

**Deliverables**
- Documentation
- FPGA bit file for companion FPGA
- Schematics, netlist and bill of materials
- Utility to reprogram the Companion FPGA configuration Flash with RealView ICE or the USB debugger integrated on RealView baseboards
- Boot monitor software
  - System Configuration
  - NOR Flash utility
  - Retarget of C I/O libraries
  - File system on multimedia card
- Self Test software
  - Checks that hardware is functional
  - Peripheral driver example
- Example software
  - Access to PCI system
  - Network Flash Utility

**Information available**

When ARM releases new development boards a large amount of information is made available at the ARM website (www.arm.com), including user guide and datasheet, board schematics, netlist and list of materials, application notes, bug fixes and lists of frequently asked questions.

**Example System: Platform Baseboard for ARM1176JZF-S and Logic Tile**

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The ARM® RealView® family of feature rich development boards provides an excellent environment for prototyping system-on-chip designs. Through a range of plug-in options, hardware and software applications can be developed and debugged.

The high performance Versatile family enhances the end-user experience for benchmarking and application development. It simplifies hardware and software development, which shortens time to market.

The Platform Baseboard for ARM11 MPCore is a development board especially designed for Symmetric Multi-Processing applications development. Performance analysis, Operating System porting and custom peripheral driver development for SMP platforms is hence enabled.

**Platform Baseboard for ARM11 MPCore**

The Platform Baseboard for ARM11 MPCore features an ARM11MPCore Test Chip with 4 ARM11MPCore CPUs, a snoop control unit and 1MB of Level 2 cache. A structured ASIC handles the high speed peripherals (DDR DMC, NOR SMC, PCI-X, AXI bus matrix) and a companion Xilinx Virtex-4 FPGA handles the low speed peripherals.

The ARM11MPCore Test Chip and the structured ASIC are connected via a non multiplexed 64bit AXI bus to give the highest possible data transfer between the two chips. The platform performance allows software development at near real time.

Using the Tile and PCI (PCI-X, PCI Express) connectors, custom peripherals can be added to the system so as to model the final product.

In order to accelerate software development and reduce time to market the Platform Baseboard is delivered with FPGA bit file and example software. A number of operating systems, including SMP Linux will also be ported to this board to help users accelerate the development of SMP OS-based applications.
Specification

Platform Baseboard Features

- ARM11 MPCore Test Chip, Structured ASIC Chip
- Virtex-4 XC4VLX40 FPGA
- 512MB DDR SDRAM, 2MB RAM
- 128MB NOR Flash
- FISMO expansion site (www.pismoworld.org)
- Tile Connector
- PCI-X and PCI-Express slots
- Standard frequency: ARM11MPCore Test Chip 200MHz, Internal AXI 70-100MHz, Expansion AXI 30MHz

Platform Baseboard Peripherals

- 10/100 Ethernet MAC, High Speed OTG USB v2.0 controller
- 64-bit 66MHz PCI-X controller
- 100MHz 32-bit DDR SDRAM controller
- 50MHz 32-bit Asynchronous SRAM controller
- 50MHz 32-bit NOR Flash controller
- VGA/DVI, Keyboard and mouse connectors
- SmartCard and Multimedia/SD Card controller, Compact Flash Interface
- Stereo audio Line in/out and microphone
- 4 UARTs and character LCD
- Switches, LEDs and GPIO headers

Note: Speed figures subject to change

Deliverables

- Documentation
- FPGA bit-file for Companion FPGA
- Schematics, netlist and bill of materials
- Utility to reprogram the Companion FPGA configuration Flash with RealView ICE or the USB debugger integrated on RealView baseboards
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  o System Configuration
  o NOR Flash utility
  o Retarget of C I/O libraries
- Self Test software
  o Checks that hardware is functional
  o Peripheral driver example
- Example software
  o Access to PCI system
  o Network Flash Utility

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Example System: Platform Baseboard for ARM11 MPCore and Logic Tile

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The high performance Versatile family enhances the end-user experience for benchmarking and application development. It simplifies hardware and software development, which shortens time to market.

The Platform Baseboard for Cortex-A8 is a development board especially designed for ARMv7 architecture applications development. Cortex-A8 processor evaluation, Operating System porting and custom peripheral driver development is hence enabled.

**Platform Baseboard for Cortex-A8**

The Platform Baseboard for Cortex-A8 features a Cortex-A8 Test Chip with NEON technology and integrated 32K Level 1 and 256K level 2 of cache. A structured ASIC handles the high speed peripherals (DDR DMC, NOR SMC, PCI, AXI bus matrix), a companion Xilinx Virtex-4 FPGA handles the standard I/O peripherals and a debug Xilinx Virtex-5 FPGA implement the CoreSight technology facilitating processor debug and trace.

The Cortex-A8 Test Chip and the structured ASIC are connected via a non multiplexed 64bit AXI bus to give the highest possible data transfer between the two chips. The platform performance allows software development at near real time.

Using the Tile and PCI (PCI, PCI Express) connectors, custom peripherals can be added to the system so as to model the final product.

In order to accelerate software development and reduce time to market the Platform Baseboard is delivered with FPGA bit file and example software. A number of operating systems, including Linux will also be ported to this board to help users accelerate the development of OS-based applications.
### Specification

**Platform Baseboard Features**
- Cortex-A8 Test Chip, Structured ASIC Chip
- SouthBridge Virtex-4 XC4VLX40 FPGA
- Debug Virtex-5 XC5VLX50T FPGA
- 512MB DDR SDRAM, 2MB Cellular RAM
- 128MB NOR Flash
- PISMO expansion site (www.pismoworld.org)
- Tile Connector
- PCI and PCI-Express slots
- *Standard frequency: Cortex-A8 Test Chip 750MHz, Internal AXI 100MHz, Expansion AXI 30MHz
- PB-A8 is Micro ATX, self-powered, supplied in a case

*speed figures subject to change*

**Platform Baseboard Peripherals**
- 10/100 Ethernet MAC, High Speed OTG USB v2.0 controller
- 32-bit 66MHz PCI controller
- 100MHz 32-bit DDR SDRAM controller
- 50MHz 32-bit Asynchronous SRAM controller
- 50MHz 32-bit NOR Flash controller
- VGA/DVI, Keyboard and mouse connectors
- SmartCard and Multimedia/SD Card controller, Compact Flash Interface
- Stereo audio Line in/out and microphone
- 4 UARTs
- Switches, LEDS and GPIO headers

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- Documentation
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- Boot monitor software
  - System Configuration
  - NOR Flash utility
- Retarget of C I/O libraries
- Example software
  - Access to PCI system
  - Network Flash Utility
  - Linux Debian 2.6.19 patch, BSP

**Information available**
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**PB-A8 Datasheet v1.1**